Code.No: RR410506 | RR | SET-1

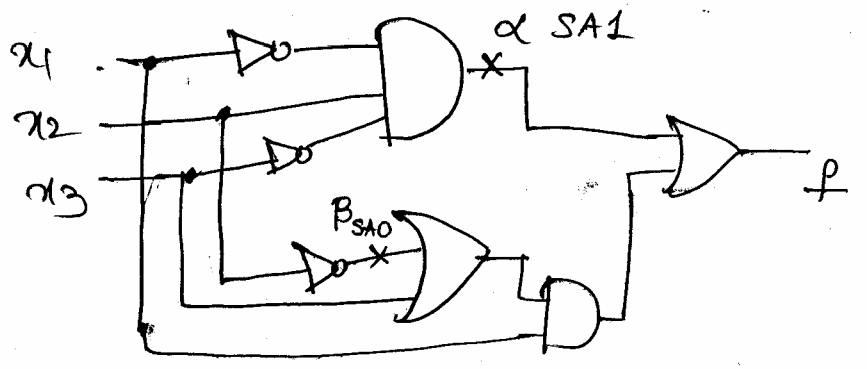
IV B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
FAULT TOLERANT SYSTEMS
(COMMON TO CSE, ECC)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1. a) What is meant by Reliability? Derive an expression for Reliability of a system in times of constant fault rate λ.
   b) A system has about 1, 00,000 components each with a facture rate of 0.75% per 1000 hours. What is the period of 0.98 reliability of this system. [8+8]

2. Design a 4 bit Line as feedback shift register to generate a signature to test the given circuit for the stuck at faults indicated below. [16]



3. a) Show that simplex system has better reliability factor than a TMR in the presence of one faulty module.
   b) Design a sift out modular redundant system of 4 channels. [8+8]

4. a) Explain how a Hybrid (3,S) system is better than a static and dynamic systems. Derive an expression for R(t) of hybrid system. Extend the same for (N, S) system.
   b) Write a brief role on software redundancy techniques. [8+8]

5. a) Design a totally self checking checker circuit proposed by Mawf and Friedman for a m out of n code.
   b) Explain the principle of operation of strongly fault secure circuit with an example. [8+8]

6. Design a totally self checking checker circuit using PLA for the given multi input and multi out put circuit.
   $f_1(A,B,C,D) = \sum (1,2,4,7,8,11,13)$
   $f_2(A,B,C,D) = \sum (0,4,5,6,9,10,14)$
   $f_3(A,B,C,D) = \sum (2.3.7.9.11.14.15)$
   $f_4(A,B,C,D) = \sum (1,5,7,9,11,13)$ [16]

7. a) List out the properties of a Design for testable circuit.
   b) Obtain the list pattern for the given Boolean expression using control logic where five tests are sufficient to detect all faults in this circuit.
   f(A,B,C,D) = $A\overline{B} + \overline{A}B\overline{C}$ + BD. [8+8]

8. a) What are the advantages of LSSD technique?
   b) Draw the logic diagram of Hazard free polarity hold latch and explain its flow table and excitation table.
   c) Write a brief note on Build in self test. [5+5+6]

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Code.No: RR410506 | RR | SET-2

IV B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
FAULT TOLERANT SYSTEMS
(COMMON TO CSE, ECC)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1. a) Show that simplex system has better reliability factor than a TMR in the presence of one faulty module.
   b) Design a sift out modular redundant system of 4 channels. [8+8]

2. a) Explain how a Hybrid (3,S) system is better than a static and dynamic systems. Derive an expression for R(t) of hybrid system. Extend the same for (N, S) system.
   b) Write a brief role on software redundancy techniques. [8+8]

3. a) Design a totally self checking checker circuit proposed by Mawf and Friedman for a m out of n code.
   b) Explain the principle of operation of strongly fault secure circuit with an example. [8+8]

4. Design a totally self checking checker circuit using PLA for the given multi input and multi out put circuit.
   $f_1(A,B,C,D) = \sum (1,2,4,7,8,11,13)$
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   $f_4(A,B,C,D) = \sum (1,5,7,9,11,13)$ [16]

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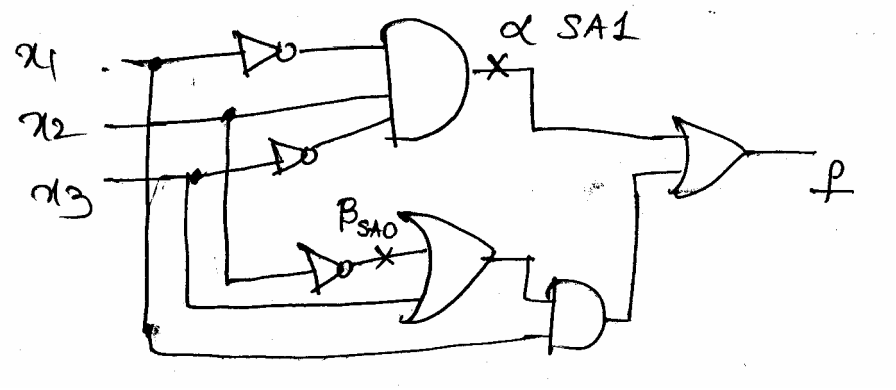
   b) Obtain the list pattern for the given Boolean expression using control logic where five tests are sufficient to detect all faults in this circuit.
   $f(A,B,C,D) = A\overline{B} + \overline{A}B\overline{C}$ +BD. [8+8]

6. a) What are the advantages of LSSD technique?
   b) Draw the logic diagram of Hazard free polarity hold latch and explain its flow table and excitation table.
   c) Write a brief note on Build in self test. [5+5+6]

7. a) What is meant by Reliability? Derive an expression for Reliability of a system in times of constant fault rate λ.
   b) A system has about 1, 00,000 components each with a facture rate of 0.75% per 1000 hours. What is the period of 0.98 reliability of this system? [8+8]

8. Design a 4 bit Line as feedback shift register to generate a signature to test the given circuit for the stuck at faults indicated below. [16]



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Code.No: RR410506 | RR | SET-3

IV B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
FAULT TOLERANT SYSTEMS
(COMMON TO CSE, ECC)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1. a) Design a totally self checking checker circuit proposed by Mawf and Friedman for a m out of n code.
   b) Explain the principle of operation of strongly fault secure circuit with an example. [8+8]

2. Design a totally self checking checker circuit using PLA for the given multi input and multi out put circuit.
   $f_1(A,B,C,D) = \sum (1,2,4,7,8,11,13)$
   $f_2(A,B,C,D) = \sum (0,4,5,6,9,10,14)$
   $f_3(A,B,C,D) = \sum (2.3.7.9.11.14.15)$
   $f_4(A,B,C,D) = \sum (1,5,7,9,11,13)$ [16]

3. a) List out the properties of a Design for testable circuit.
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4. a) What are the advantages of LSSD technique?
   b) Draw the logic diagram of Hazard free polarity hold latch and explain its flow table and excitation table.
   c) Write a brief note on Build in self test. [5+5+6]

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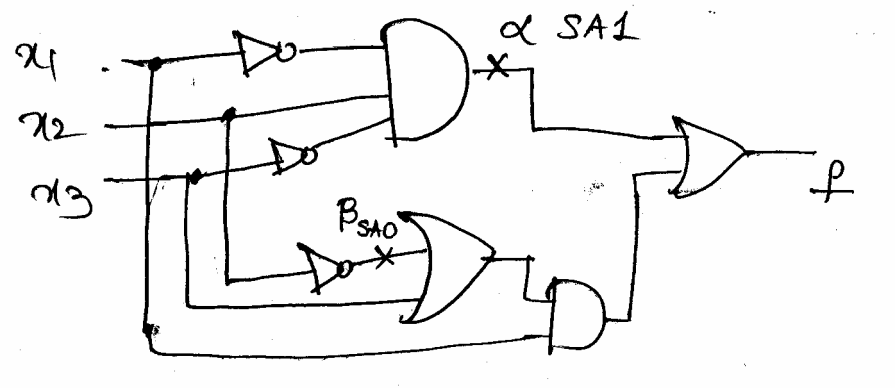

7. a) Show that simplex system has better reliability factor than a TMR in the presence of one faulty module.
   b) Design a sift out modular redundant system of 4 channels. [8+8]

8. a) Explain how a Hybrid (3,S) system is better than a static and dynamic systems. Derive an expression for R(t) of hybrid system. Extend the same for (N, S) system.
   b) Write a brief role on software redundancy techniques. [8+8]

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Code.No: RR410506 | RR | SET-4

IV B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
FAULT TOLERANT SYSTEMS
(COMMON TO CSE, ECC)

Time: 3hours **Max.Marks:80**

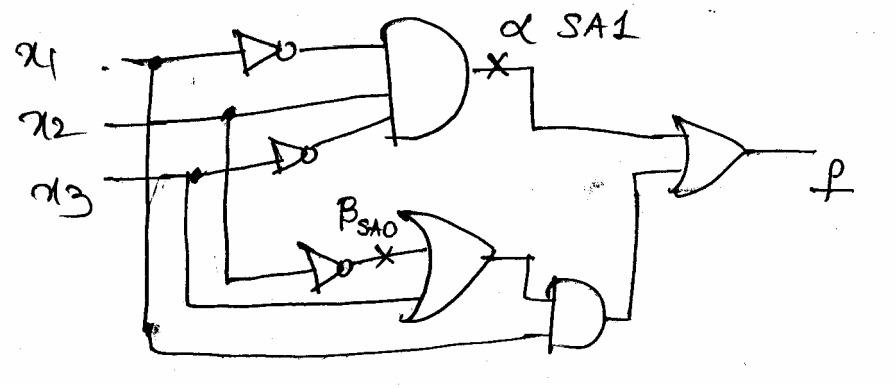
Answer any FIVE questions
All questions carry equal marks
- - -

1. a) List out the properties of a Design for testable circuit.
   b) Obtain the list pattern for the given Boolean expression using control logic where five tests are sufficient to detect all faults in this circuit.
   f(A,B,C,D) = $A\overline{B} + \overline{A}B\overline{C}$ +BD. [8+8]

2. a) What are the advantages of LSSD technique?
   b) Draw the logic diagram of Hazard free polarity hold latch and explain its flow table and excitation table.
   c) Write a brief note on Build in self test. [5+5+6]

3. a) What is meant by Reliability? Derive an expression for Reliability of a system in times of constant fault rate λ.
   b) A system has about 1, 00,000 components each with a facture rate of 0.75% per 1000 hours. What is the period of 0.98 reliability of this system? [8+8]

4. Design a 4 bit Line as feedback shift register to generate a signature to test the given circuit for the stuck at faults indicated below. [16]



5. a) Show that simplex system has better reliability factor than a TMR in the presence of one faulty module.
   b) Design a sift out modular redundant system of 4 channels. [8+8]

6. a) Explain how a Hybrid (3,S) system is better than a static and dynamic systems. Derive an expression for R(t) of hybrid system. Extend the same for (N, S) system.
   b) Write a brief role on software redundancy techniques. [8+8]

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